LISTING OF CLAIMS

1. (Original) A Content Addressable Memory (CAM) cell providing improved speed and enhanced reliability, comprising:

a data latch with complementary data terminals,

a pair of complementary data lines that provide data connectivity with the data latch during read, write and search operations,

a pair of input controlled switches that selectively couple the data latch terminals to the complementary data lines during read or write operations,

a pair of output series pass transistors, each having its control terminal connected to a separate terminal of the data latch, one of its main terminals connected to a separate bit line, and the second main terminal connected to the corresponding terminal of the other series pass transistor,

a Match Output signal line that identifies a match/no-match at the end of a Search operation,

an output controlled switch having its control terminal connected to the common main terminal of the series pass transistors, while one of its main terminals drives the Match Output signal line to provide the result of the search operation, and

a Search Enable signal line that enables the output controlled switch only during the search operation,

the arrangement being such that during the search operation neither of the output series pass transistors conducts if the complementary bit line data matches the data latch outputs, one of

the output series pass transistors conducts maximally providing a minimal voltage drop and a low impedance charging path for the bootstrap capacitance at the enabled output controlled switch when the complementary bit line data does not match the latch data, and one of the series pass transistors conducts to discharge the bootstrap capacitance at the beginning of the precharge period of the complementary bit lines.

2. (Original) A CAM cell as claimed in claim 1, wherein the output series pass transistors are P-channel MOS transistors with a relatively low threshold voltage, and the output controlled switch is an n-channel MOS transistor with a relatively high threshold voltage, and the complementary bit lines are precharged to a "high" level.

3. (Original) A method for providing a Content Addressable Memory (CAM) cell offering improved speed and enhanced reliability, comprising the steps of:

providing a data latch with complementary data terminals,

supplying a pair of complementary data lines that provide data connectivity with the data latch during read, write and search operations,

selectively coupling the data latch terminals to the complementary data lines during read or write operations,

connecting the control terminal of each of a pair of output series pass transistors to a separate terminal of the data latch, one of its main terminals to a separate bit line, and the second main terminal to the corresponding terminal of the other series pass transistor,

providing a Match Output signal line that identifies a match/no-match at the end of a Search operation,

connecting the control terminal of an output controlled switch to the common main terminal of the series pass transistors, while one of its main terminals drives the Match Output signal line to provide the result of the search operation, and

supplying a Search Enable signal line that enables the output controlled switch only during the search operation,

the arrangement being such that during the search operation neither of the output series pass transistors conducts if the complementary bit line data matches the data latch outputs, one of the output series pass transistors conducts maximally providing a minimal voltage drop and a low impedance charging path for the bootstrap capacitance at the enabled output controlled switch when the complementary bit line data does not match the latch data, and one of the series

pass transistors conducts to discharge the bootstrap capacitance at the beginning of the precharge period of the complementary bit lines.

4. (Currently Amended) A Content Addressable Memory (CAM) cell, comprising:

a 6T SRAM cell data latch circuit including true and false terminals; and

a comparison circuit comprising first and second p-channel transistors connected in series at a bit match node, a first of the p-channel transistors having its gate connected to the true terminal of the data latch circuit and a second of the p-channel transistors having its gate connected to the false terminal of the data latch circuit.

5. (Canceled).

6. (Original) The cell of claim 4 further including a true bit line and a false bit line, wherein the true bit line is connected to a conduction terminal of the first p-channel transistor and the false bit line is connected to a conduction terminal of the second p-channel transistor.

7. (Original) The cell of claim 6 wherein the true bit line is coupled through a first word line pass transistor to the true terminal of the data latch circuit and the false bit line is coupled through a second word line pass transistor to the false terminal of the data latch circuit.

8. (Original) The cell of claim 4 wherein the comparison circuit further includes a match line transistor having conduction terminals coupled between a match line and a reference line and a gate terminal coupled to the bit match node.

9. (Original) The cell of claim 8 wherein the reference line is a pulsed ground line.

10. (Currently Amended) A Content Addressable Memory (CAM) cell, comprising:

a data latch circuit including true and false terminals; and

a comparison circuit comprising first and second p-channel transistors connected in series at a bit match node, a first of the p-channel transistors having its gate connected to the true terminal of the data latch circuit and a second of the p-channel transistors having its gate connected to the false terminal of the data latch circuit, wherein the comparison circuit further includes a match line transistor having conduction terminals coupled between a match line and a reference line and a gate terminal coupled to the bit match node ~~The cell of claim 8,~~

wherein the first and second p-channel transistors have a first Vt value and the match line transistor has a second Vt value, the second Vt value being higher than the first Vt value.

11. (Original) The cell of claim 8 wherein the match line transistor is an n-channel transistor.

12. (Original) The cell of claim 6 wherein the true bit line is a search true bit line and the false bit line is a search false bit line.

13. (Currently Amended) A Content Addressable Memory (CAM) cell, comprising:

a data latch circuit including true and false terminals;

a comparison circuit comprising first and second p-channel transistors connected in series at a bit match node, a first of the p-channel transistors having its gate connected to the true terminal of the data latch circuit and a second of the p-channel transistors having its gate connected to the false terminal of the data latch circuit;

a true bit line and a false bit line, wherein the true bit line is connected to a conduction terminal of the first p-channel transistor and the false bit line is connected to a conduction terminal of the second p-channel transistor, and wherein the true bit line is a search true bit line and the false bit line is a search false bit line ~~The cell of claim 12 further including~~; and

a read/write true bit line and a read/write false bit line and wherein the read/write true bit line is coupled through a first word line pass transistor to the true terminal of the data latch circuit and the read/write false bit line is coupled through a second word line pass transistor to the false terminal of the data latch circuit.

14. (Currently Amended) A Content Addressable Memory (CAM) cell, comprising:

a data latch circuit including true and false terminals; and

a comparison circuit comprising:

first and second transistors connected in series at a bit match node, the first transistor having its gate connected to the true terminal of the data latch circuit and the second transistor having its gate connected to the false terminal of the data latch circuit; and

a match line transistor having conduction terminals coupled between a match line and a reference line and a gate terminal coupled to the bit match node;

wherein the first and second transistors have a first Vt value and the match line transistor has a second Vt value, the second Vt value being higher than the first Vt value.

15. (Original) The cell of claim 14 wherein the data latch circuit is a 6T SRAM cell.

16. (Original) The cell of claim 14 further including a true bit line and a false bit line, wherein the true bit line is connected to a conduction terminal of the first transistor and the false bit line is connected to a conduction terminal of the second transistor.

17. (Original) The cell of claim 16 wherein the true bit line is coupled through a first word line pass transistor to the true terminal of the data latch circuit and the false bit line is coupled through a second word line pass transistor to the false terminal of the data latch circuit.

18. (Original) The cell of claim 16 wherein the true bit line is a search true bit line and the false bit line is a search false bit line.

19. (Original) The cell of claim 18 further including a read/write true bit line and a read/write false bit line and wherein the read/write true bit line is coupled through a first word line pass transistor to the true terminal of the data latch circuit and the read/write false bit line is coupled through a second word line pass transistor to the false terminal of the data latch circuit.

20. (Original) The cell of claim 14 wherein the first and second transistors are p-channel transistors and the match line transistor is an n-channel transistor.

21. (Original) The cell of claim 14 wherein the reference line is a pulsed ground line.